ABSTRACT

The clock generator of this invention saves a buffer memory for the data transfer interface, which has conventionally been required, when using a spectrum spread clock in circuits and devices inside a system. The clock generator can easily be applied as the operational clock in a system, and enhances the performance of the system. In the clock generator, the variable delay circuit controls the phase of the reference clock generated by an oscillator. The delay setting circuit is able to vary the setting of the control voltage to the variable delay circuit at each clock cycle, and modulates the phase of the reference clock. The phase modulation means of the delay setting circuit fluctuates the cycle of the output modulation clock to thereby spread the spectrum. Also, the delay setting circuit detects the output states (edges of the clock) of delay elements of the variable delay circuit, and confines the phase difference of the reference clock and the modulated clock within a specified range (for example, half the cycle of the reference clock). Thereby, the clock generator guarantees a certain extent of synchronization in the spectrum spread clock.